Syntax		Description	Status Affected
addlw	**number**	**add**s a **number** to the number in the **w**orking register.	C, DC, Z
addwf	**FileReg, dest**	**add**s the **w**orking register to the number in a **f**ile register and puts the result in **dest**.	C, DC, Z
andlw	**number**	**AND**s a **number** with the working register, leaving the result in the working register.	Z
andwf	**FileReg, dest**	**AND**s the **w**orking register with the number in the **f**ile register	Z
bcf	**FileReg, bit**	**c**lears a **b**it in a **f**ile register	None
bsf	**FileReg, bit**	**s**ets a **b**it in **f**ile register	None
btfsc	**FileReg, bit**	**t**ests a **b**it in a **f**ile register and skips the next instruction if the result is clear	None
btfss	**FileReg, bit**	**t**ests a **b**it in a **f**ile register and skips the next instruction if the result is set	None
call	**Sub**	**Call** a **sub**routine.	None
clrf	**FileReg**	**cl**ea**r**s the **f**ile register.	Z
clrw		**cl**ea**r**s the **w**orking register.	Z
clrwdt		**cl**ea**r**s the **w**atch**d**og **t**imer.	/TO, /PD
comf	**FileReg, dest**	**com**plements (inverts) the **f**ile register.	Z
decf	**FileReg, dest**	**dec**rements a **f**ile register.	Z
decfsz	**FileReg, dest**	**dec**rements a **f**ile register and **s**kip next instruction if result is **z**ero.	None
goto	**label**	**Go to** the label	None
incf	**FileReg, dest**	**inc**rements a **f**ile register.	Z
incfsz	**FileReg, dest**	**inc**rements a **f**ile register and skip next instruction if result is **z**ero.	None
iorlw	**number**	inclusive **OR**s a **number** with the **w**orking register	Z
iorwf	**FileReg, dest**	inclusive **OR**s the **w**orking register with the number in a **f**ile register.	Z
movfw	**FileReg**	**mov**es (copies) the number in a **f**ile register into the **w**orking register. **movf FileReg, w** is equivalent.	Z
movlw	**number**	**mov**es (copies) a **number** (literal) into the **w**orking register.	None
movwf	**FileReg**	**mov**es (copies) the number in a **w**orking register into the **f**ile register.	None
nop		**n**o **op**eration.	None
option		moves the number in the working register into the **option** register. *16C5X only*	None
retfie		**ret**urns **f**rom subroutine and set the Global **I**nterrupt **E**nable bit.	None
retlw	**number**	**ret**urns from a subroutine with a particular **number** (**l**iteral) in the **w**orking register	None
return		**return**s from a subroutine	None
rlf	**FileReg, dest**	**r**otates the bits in a **f**ile register to the **l**eft	C
rrf	**FileReg, dest**	**r**otates the bits in a **f**ile register to the **r**ight	C
sleep		makes the PIC sleep (low-power-mode)	/TO, /PD
sublw	**number**	**sub**tracts the **w**orking register from a **number**	C, DC, Z
subwf	**FileReg, dest**	**sub**tracts the **w**orking register from the number in **f**ile register.	C, DC, Z
swapf	**FileReg, dest**	**swaps** the two nibbles of the **f**ile register.	None
tris	**PORTX**	uses the number in the working register to specify which bits of a port are inputs (1) and outputs (0). *16C5X only*	None
xorlw	**number**	e**x**clusive **OR**s a **number** with the **w**orking register	Z
xorwf	**FileReg, dest**	e**x**clusive **OR**s the **w**orking register with the **f**ile register.	Z

Register File Map - PIC16F84

	Bank 0	Bank1	
00h	Indirect addr	Indirect addr	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h			87h
08h	EEDATA	EECON1	88h
09h	EEADR	EECON2	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	68 General Purpose registers (SRAM)	Mapped in Bank 0	8Ch
4Fh			CFh
50h			D0h
7Fh			FFh

STATUS Register (03h, 83h)

IRP	RP1	RP0	/TO	/PD	Z	DC	C

bit 7: **IRP**: Register select bank.
0 = Bank 0, 1 (00h - FFh)
1 = Bank 2, 3 (100h,1FFh)

bit 6-5: **RP1:RP0:** Register Bank Select bits.
00 = Bank 0 (00h - 7Fh)
01 = Bank 1 (80h - FFh)
10 = Bank 2 (100h - 17Fh)
11 = Bank 3 (180h - 1FFh)
Only RP0 used by PIC16F84

bit 4: **/TO**: Time-out bit.
1 = After power-up, `CLRWDT` or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: **/PD**: Power-down bit.
1 = After power-up or by the `CLRWDT` instruction.
0 = By execution of the `SLEEP` instruction.

bit 2: **Z**: Zero bit.

bit 1: **DC**: Digit carry/borrow bit (for `ADDWF` and `ADDLW` instructions)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0: **C**: Carry/borrow bit.

OPTION Register (81h)

/RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0

bit 7: **/RBPU**: PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled

bit 6: **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5: **TOCS**: TMR0 Clock Source Select bit
1 = Transition on RA4/TOCKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **TOSE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/TOCKI pin
0 = Increment on low-to-high transition on RA4/TOCKI pin

bit 3: **PSA**: Prescaler Assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to TMR0

bit 2-0: **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

INTCON Register (0Bh, 8Bh)

GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF

bit 7: **GIE**: Global Interrupt Enable bit.
1 = Enables all un-masked interrupts
0 = Disables all interrupts

bit 6: **EEIE**: EE Write Complete Interrupt Enable bit.
1 = Enables the EE write complete interrupt
0 = Disables the EE write complete interrupt

bit 5: **T0IE**: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4: **INTE**: RB0/INT Interrupt Enable bit
1 = Enables the RB0/INT interrupt
0 = Disables the RB0/INT interrupt

bit 3: **RBIE**: RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: **T0IF**: TMR0 overflow interrupt flag bit
1 = TMR0 has overflowed
0 = TMR0 did not overflow

bit 1: **INTF**: RB0/INT Interrupt Flag bit
1 = The RB0/INT interrupt occurred
0 = The RB0/INT interrupt did not occur

bit 0: **RBIF**: RB Port Change Interrupt Flag bit
1 = When at least one of the RB7:RB4 pins changed state
0 = None of the RB7:RB4 bits have changed state

NB: Bits 0 to 2 *must* be cleared in software before re-enabling interrupts!